This listing of claims replaces all prior listings:

1. (currently amended) An apparatus, said apparatus comprising:

a semiconductor device including a central processing unit (CPU) and a read control circuit (RCC); ~~and~~

a data-rewritable nonvolatile memory communicatively coupled to the CPU that includes a plurality of data blocks with each data block including a plurality of data pages, ~~said data-rewritable nonvolatile memory having a plurality of data blocks wherein boot program instructions are stored in parallel, said boot program instructions comprising a plurality of pages of data, each said page being stored in parallel in at least two data blocks,~~

wherein,

~~said semiconductor device comprising a central processing unit (CPU) and a read control circuit (RCC), wherein:~~

at least two boot program instructions are stored in a predetermined number of data blocks in parallel in the data-rewritable nonvolatile memory, the predetermined number being less than the total number of data blocks,

block state information indicating that a data block is faulty or not faulty is stored in a leading data page of each of the data blocks storing boot program instructions,

the CPU is configured, in part, to specify to the RCC a read position for reading out ~~each page of~~ the boot program instruction ~~instructions~~ from a data block ~~stored~~ in the data-rewritable nonvolatile memory at [[the]] a starting time, ~~said each page being stored in parallel in at least a first respective data block and a second respective data block~~; and

the RCC is configured to (a) determine whether the first respective data block is faulty or not according to ~~first data read out from the first respective data block~~the block state information, (b) output the first data to the CPU when the first data block is determined as not faulty, and (c) read, when the first respective data block is determined as faulty, second data from the second respective data block and output said second data to the CPU when said second respective data block is determined as not faulty, and

~~wherein,~~

the RCC prevents the CPU from accessing the data-rewritable non volatile memory while the RCC determines which data block to output to the CPU.

2. (previously presented) The apparatus of claim 1, wherein the read control circuit is configured to determine whether a data block is faulty or not faulty at least according to an error correction code contained in the data read out from the data-rewritable nonvolatile memory.

3. (previously presented) The apparatus of claim 2, wherein the RCC corrects the data and supplies said data to the CPU when said RCC determines that the data is correctable according to the error correction code but otherwise determines that the data block is faulty when it determines that the data is uncorrectable data.

4. (currently amended) The apparatus of claim 1, wherein the RCC is configured to determine that a data block is faulty or not faulty at least according to [[a]] the block state information contained in the data read out from the data-rewritable nonvolatile memory.

5. (previously presented) The apparatus of claim 4, wherein the RCC determines that the block is faulty when the block state information does not show a predetermined value.

6. (cancelled)

7. (previously presented) The apparatus of claim 1, wherein the data-rewritable nonvolatile memory is a NAND type flash memory.

8. (currently amended) A processing method for starting up a semiconductor device, said device comprising a central processing unit (CPU) and a read control circuit (RCC), said CPU configured, in part, to start by reading out boot program instructions from a data-rewritable nonvolatile memory, said data-rewritable nonvolatile memory ~~having a plurality of data blocks wherein boot program instructions are stored in parallel,~~ is communicatively coupled to the CPU and including a plurality of data blocks with each data block including a plurality of data pages ~~said boot program instructions comprising a plurality of pages of data, each said page being stored in parallel in at least two data blocks~~, the processing method comprising the steps of:

~~the CPU~~ specifying to the RCC, by the CPU, a read position for reading out ~~each page of~~ the boot program instructions stored in a first data block in the data-rewritable nonvolatile memory, ~~said each page being stored in parallel in at least a first respective data block and a second respective data block~~; and

~~the RCC~~ determining, via the RCC, whether the first ~~respective~~ data block is faulty or not by reading ~~according to first data~~block state information stored in a leading data page of the first data block that indicates whether the data block is faulty or not faulty ~~read out from the first respective data block~~; and

outputting ~~the~~ a first data from the first data block to the CPU when the first data block is determined as not faulty, and reading, when the first ~~respective~~ data block is determined as faulty, second data from [[the]] ~~second respective~~ a second data block and outputting said second data to the CPU when ~~said~~ a block state information stored in a leading data page of the second data block indicates that the second data block is not faulty~~second respective data block is determined as not faulty~~,

wherein,

at least two boot program instructions are stored in a predetermined number of data blocks in parallel in the data-rewritable nonvolatile memory, the predetermined number being less than the total number of data blocks, and

the RCC prevents the CPU from accessing the non-volatile memory while the RCC determines the data block to output to the CPU.